When the integrated circuit device 21 is mounted on a printed circuit board, the input buffer circuit 1 receives the input signal IN having a full amplitude. Accordingly, the transfer circuit 4A is used in the normal usage. The input buffer circuit 1 receives an input control signal St high via a pad P2. As a result, a control signal /St low is supplied to the gates of the NMOS transistors Tn4 and Tn5 and the PMOS transistors Tp3-Tp5 of Fig. 2. The transfer circuit 4A is enabled and the input operation for the full-amplitude input signal IN is carried out with low power consumption.

Switch SW1 is closed while switch SW2 is open.

Please replace page 15, paragraph 4 (lines 1-6) with:

That is, in operational test mode, the proper operational test on the output buffer circuit 23 is performed by enabling the differential amplifier circuit 2. When a user uses the input/output buffer circuit 22, on the other hand, the consumed power of the input buffer circuit 1 is reduced by enabling the transfer circuit 4A. In the case

IN THE CLAIMS:

Please cancel claims 11-16 without prejudice or disclosure.

Please add new claims 19-42 as follows:

19. An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an